ABOUT WAFER SPACE

Wafer Space was founded with the ideals of providing true value in Design Services to our clients in the Semiconductor and the Embedded Industry. Our world - class engineering team with its intensive knowledge in chip design and embedded systems combined with our ability to execute complex turnkey projects with a steadfast focus on quality is what differentiates us.

Wafer Space has a very rigorous selection criteria for engineers which results in a world class engineering team. We strongly believe in continuous learning and growth for all employees. Our organizational culture nurtures creativity and innovation amongst our team players as work no longer is a chore. It's what we have fun doing!

Wafer Space has design centers in Bangalore, India and California, USA. With our proactive client and employee model, Wafer Space is well positioned to deliver quality and timely services to our clientele across a wide range of high-tech markets.

Come See the Wafer Space Difference.

CONTACT US

INDIA DESIGN CENTER

MONARCH RAMANI, 7th 'C' MAIN ROAD, 1st 'A' BLOCK KORAMANGALA, BANGALORE - 560034 INDIA Tel: +91-080-46720000

US DESIGN CENTER

#2880 Zanker Road, Suite 203, San Jose, CA, 95134 USA TEL: +1 - 408 625 7195

FOR MORE INFORMATION

WEBSITE: www.waferspace.com SALES: sales@waferspace.com INFO: info@waferspace.com



wafer space



Engineering Long-term Partnerships!

WWW.WAFERSPACE.COM WWW.WAFERSPACE.COM WWW.WAFERSPACE.COM

RTL DESIGN and VERIFICATION SERVICES

RTL Design and Verification

Spec Creation, RTL Design.

Coverage Driven Test Planning, Schedule Creation.

Configurable Environment Architecture Using SV, OVM, UVM, VMM or eRM.

Low Power and Mixed Signal Verification.

Static Formal Verification.

Verification Intellectual Property (VIP) Development

OVM, UVM, VMM, eRM Based VIP's. Custom VIP Development.

Verification Methodology Consulting

Testbench Migration to UVM/OVM/VMM.

Migration to System Verilog Based Verification.

Low Power and Mixed Signal Verification.

 $Building\,Configurable\,Test benches.$

DESIGN IMPLEMENTATION SERVICES

Physical Implementation

Synthesis, Static Timing Analysis and Formal Verification.

Hierarchical Floorplanning, Partitioning, Pin Placement, Time Budgeting and Power Push Down. Placement, Clock Tree Synthesis, Routing, Signal Integrity and ECOs.

THE WAFER SPACE DIFFERENCE



Focus on Client Success

- 100% Client Satisfaction.
- Delivering True Long Term Value.
- Building Long Term Win-Win Relationships.

Have a Great Time! Remember: if it isn't fun it isn't working

Organizational Culture

- Work Hard And Have Fun At Work!
- Focus on Employee Growth Plans.
- Nurturing Leaders.



Wafer Space University

- Large Knowledge Base of Training Material.
- Technical and Leadership Training.



World Class Engineering Team

- Nurturing the Best Engineering Talent.
- Highly Experienced Team.
- Rigorous Selection Process.



Project Management Expertise

- Past Experience Managing Multiple Client Projects.
- Experience Running Offshore Design Centers (ODC) for Remote Clients.

DESIGN IMPLEMENTATION SERVICES

Signoff Timing, Extraction and Physical Verification Closure.

Expertise in Latest Nodes up to 22 nm.

Top Level (Flip Chip and Wire Bond),

Hierarchical, Low Power and Block Level

Implementation Expertise.

Design for Test (DFT)

Scan Insertion, JTAG, ATPG and Memory BIST.

EMBEDDED DESIGN SERVICES

Domains

Telecom/Networking.

Consumer Electronics.

Automotive.

Semiconductor.

Industrial Automation.

Medical Devices.

Defense & Aerospace.

Office Automation.

Services.

Board and FPGA Designs.

BSP and Firmware Development.

Embedded Application Development.

Integration of 3rd Party Solutions.

Verification and Validation.

Product Prototyping.

 $Product\,Life\,Cycle\,Support\,Solution.$